FIG 1

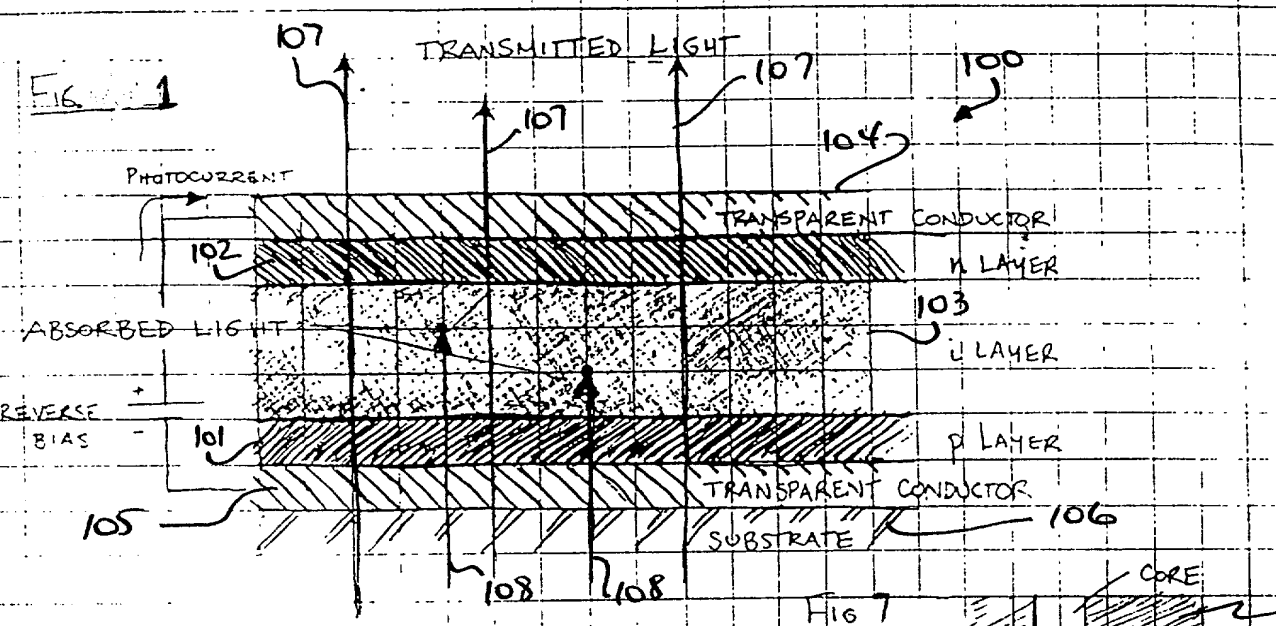


FIG 4

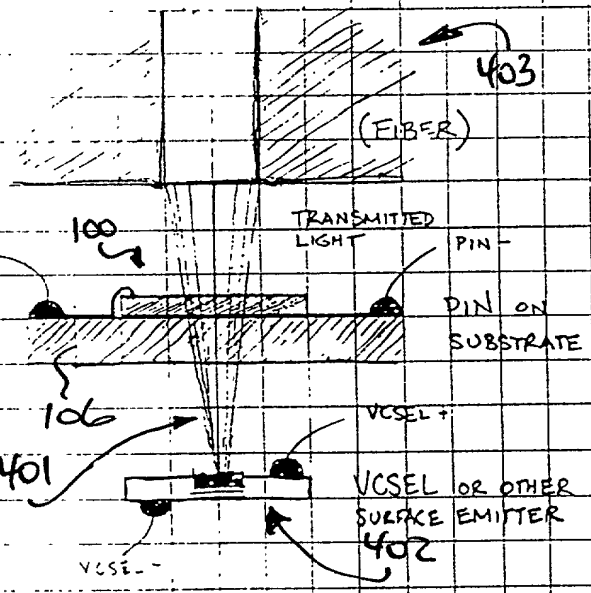


FIG 7

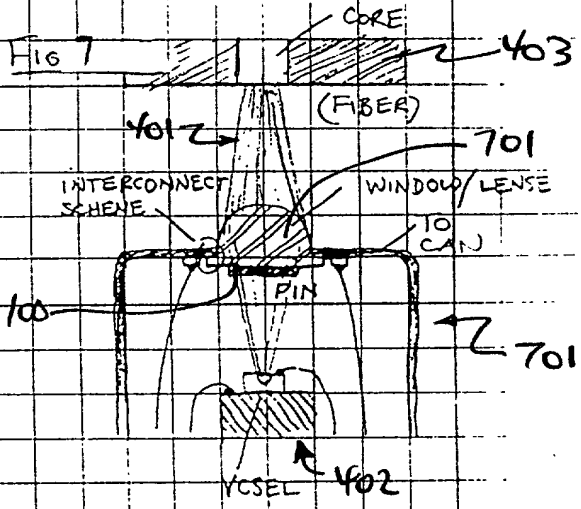


FIG 5

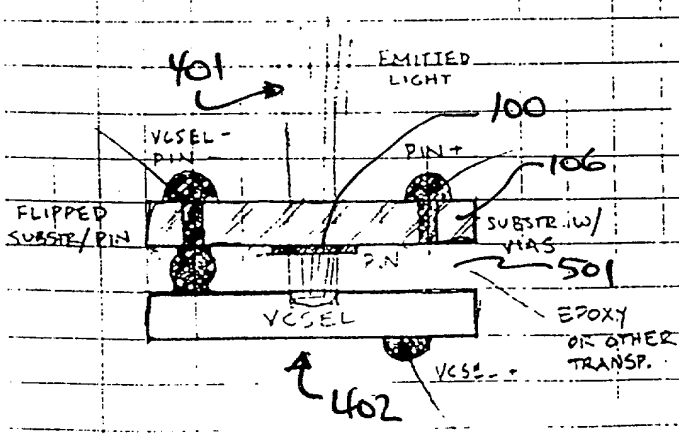


FIG 6

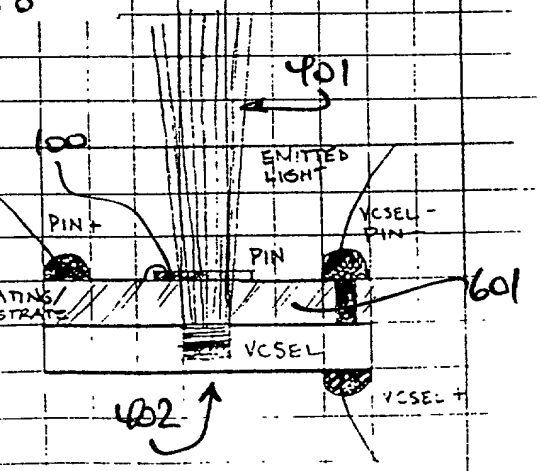


FIG 4

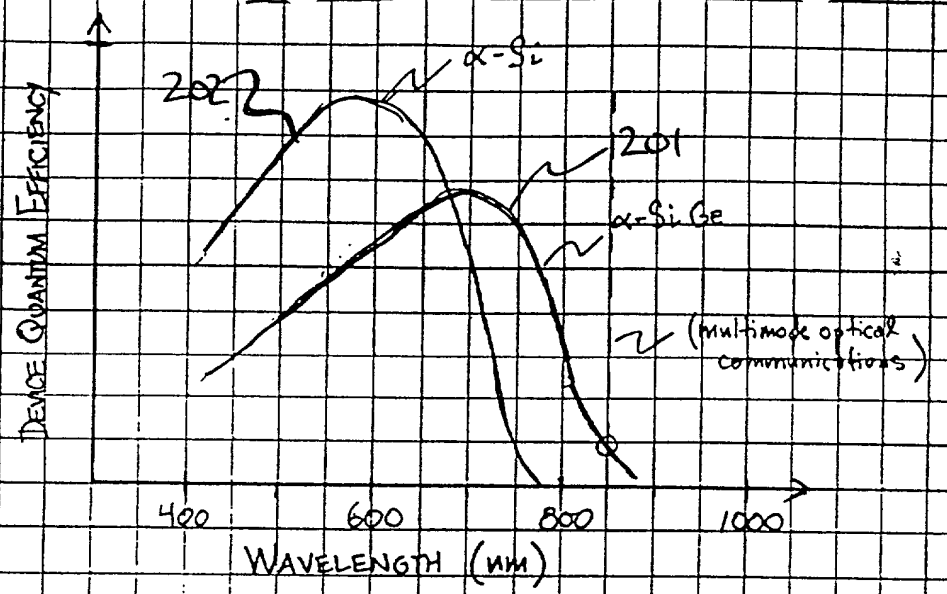

DEVICE QUANTUM EFFICIENCY
202
α-Si
201
α-Si GE
(multimode optical communications)
400
600
800
1000
WAVELENGTH (NM)

Fig. 2.

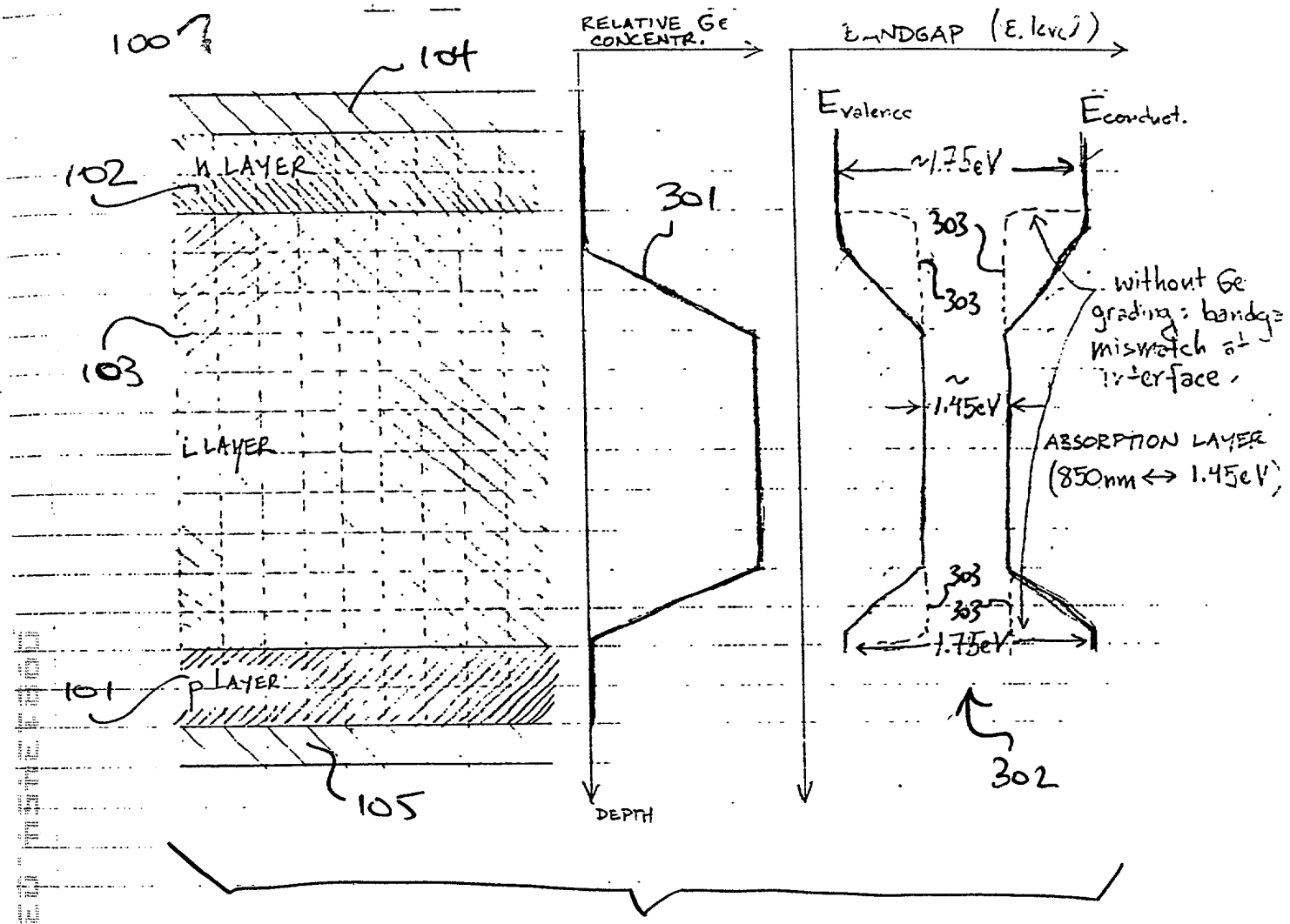

100
104
102
N LAYER
103
i LAYER
p LAYER
101
105
RELATIVE Ge CONCENTR.
DEPTH
301
BANDGAP (E. level)
E valence
E conduct.
~1.75eV
303
303
without Ge grading: bandgap mismatch at interface
~1.45eV
ABSORPTION LAYER (850nm ↔ 1.45eV)
303
303
1.75eV
302

Fig. 3

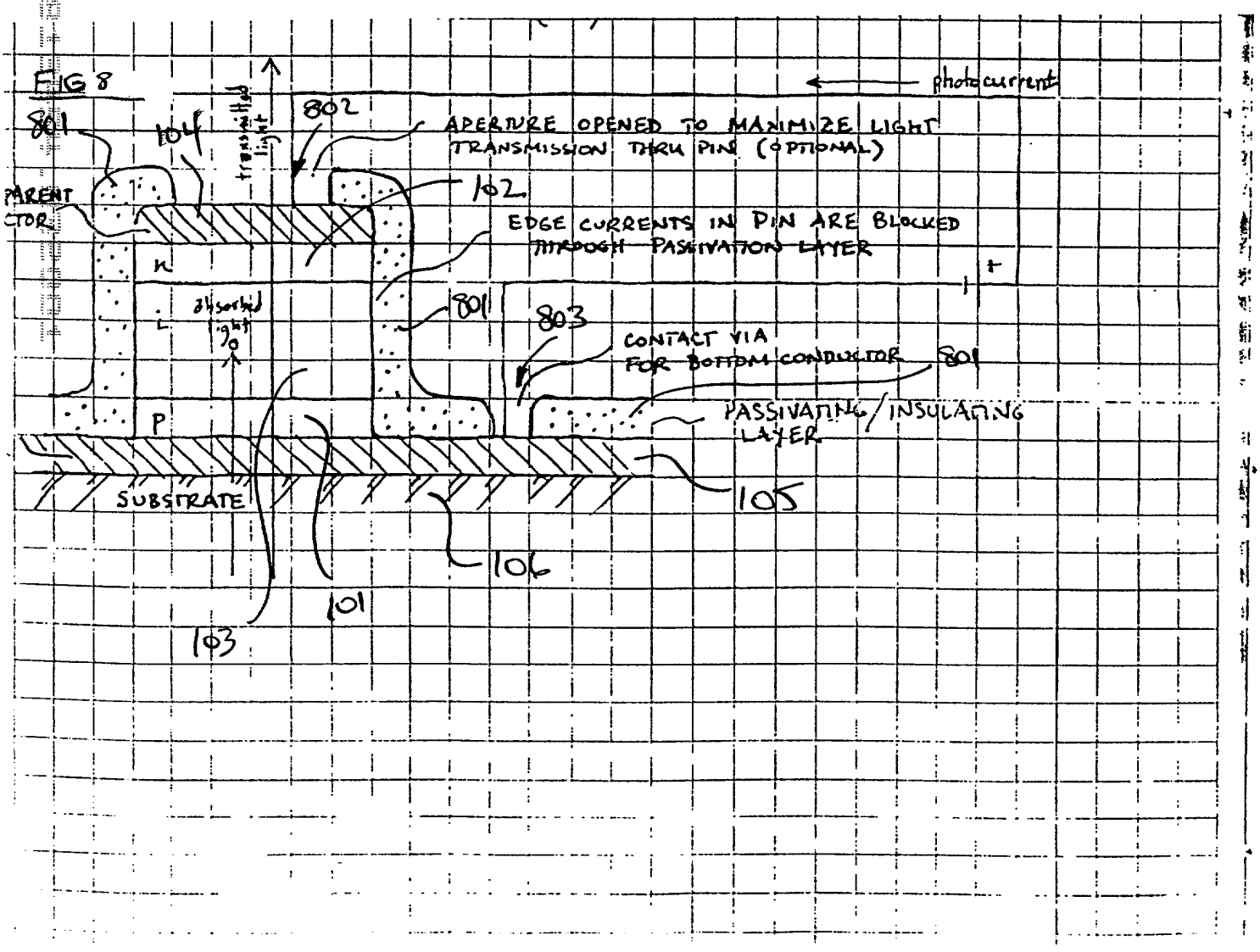


FIG 8
photocurrent
801
104
802
APERTURE OPENED TO MAXIMIZE LIGHT TRANSMISSION THRU PIN (OPTIONAL)
102
EDGE CURRENTS IN PIN ARE BLOCKED THROUGH PASSIVATION LAYER
N
801
803
CONTACT VIA FOR BOTTOM CONDUCTOR
801
P
PASSIVATING / INSULATING LAYER
SUBSTRATE
105
106
101
103

FIG 9

MOST SIMPLE STRUCTURE

- DON'T PATTERN BOTTOM T.C.
- USE TOP T.C. AS PIN ETCH MASK

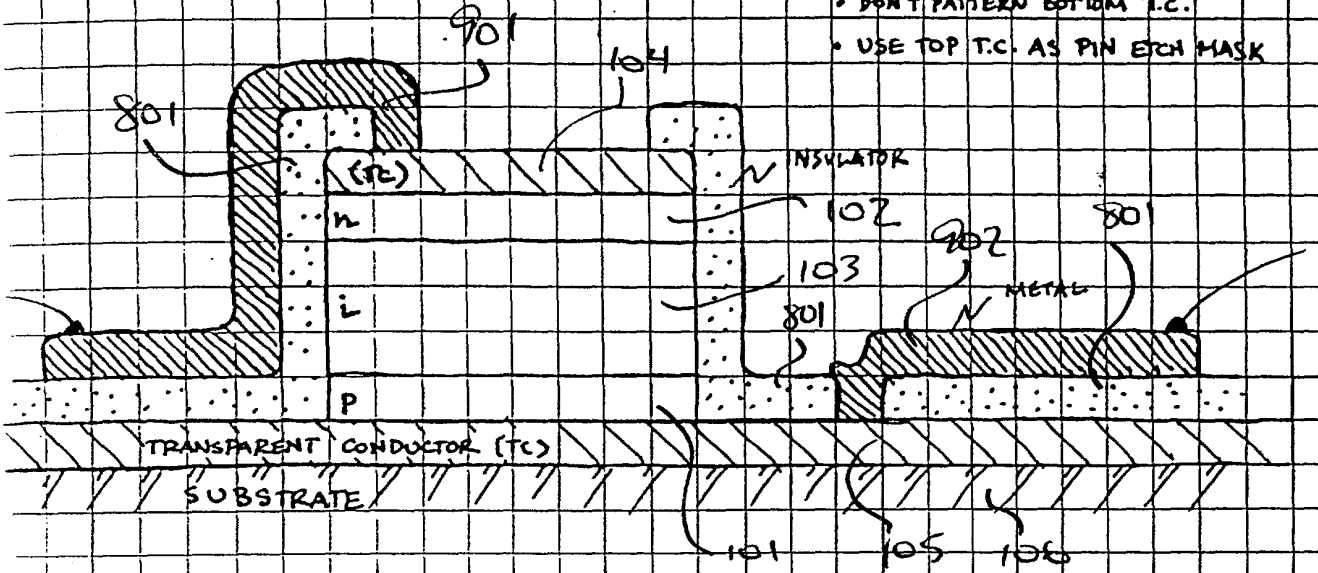


FIG 10

ADD TOP T.C. AFTER INSULATOR; SLIGHTLY LARGER APERTURE

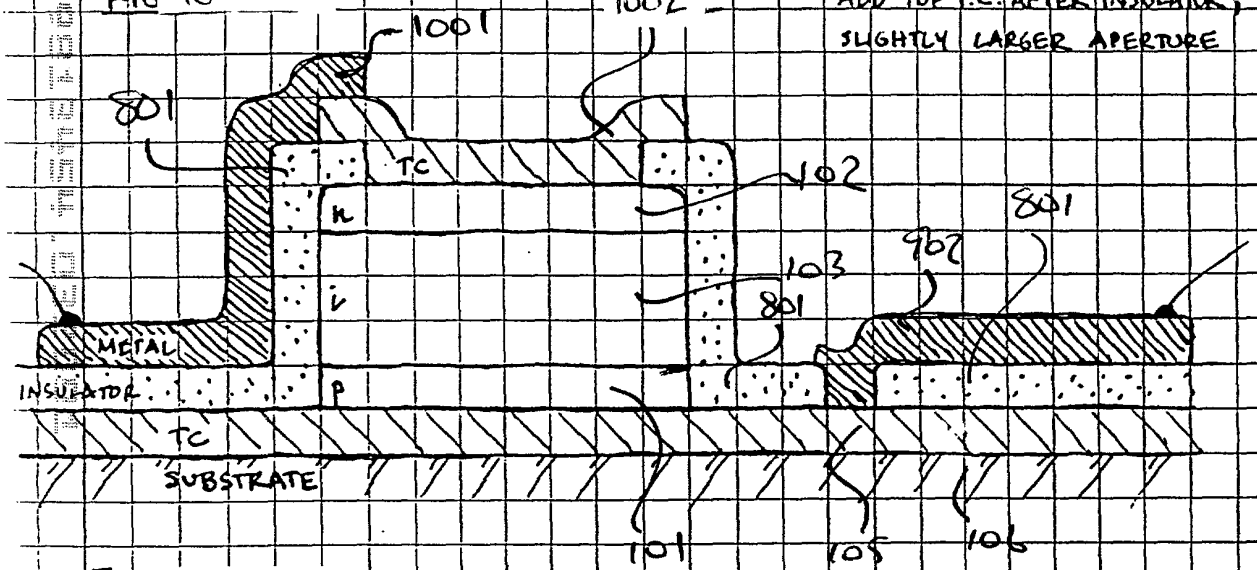


FIG 11

PATTERN BOTTOM T.C. — REDUCE CAPACITANCES

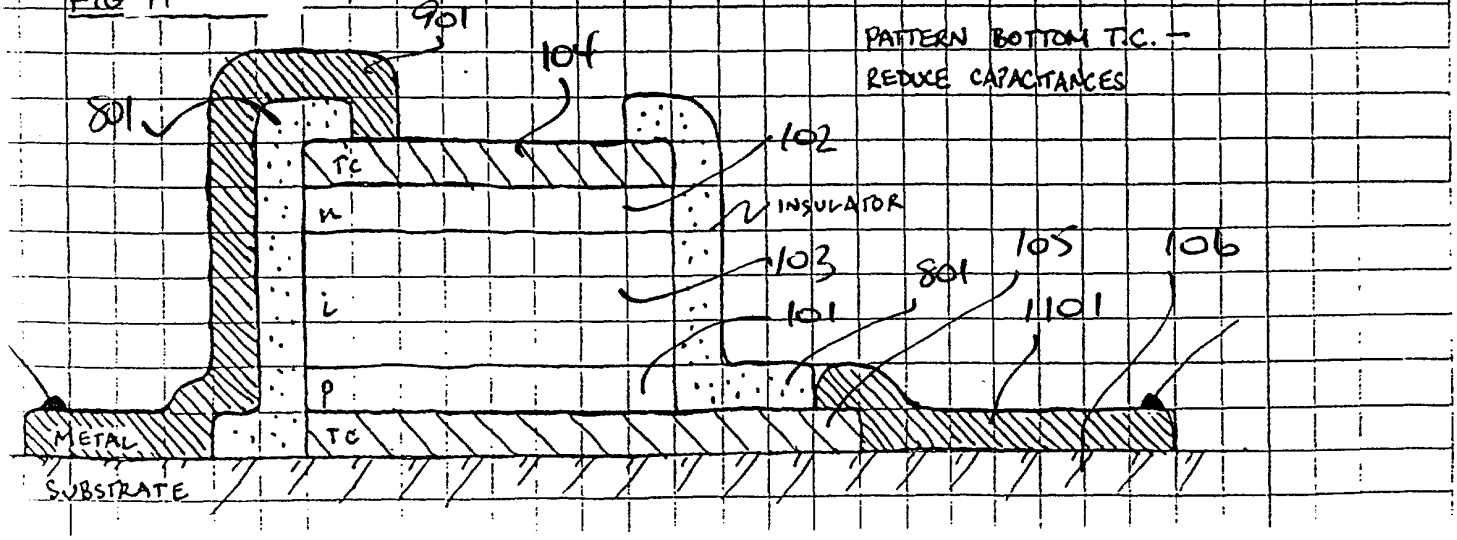


FIG. 12

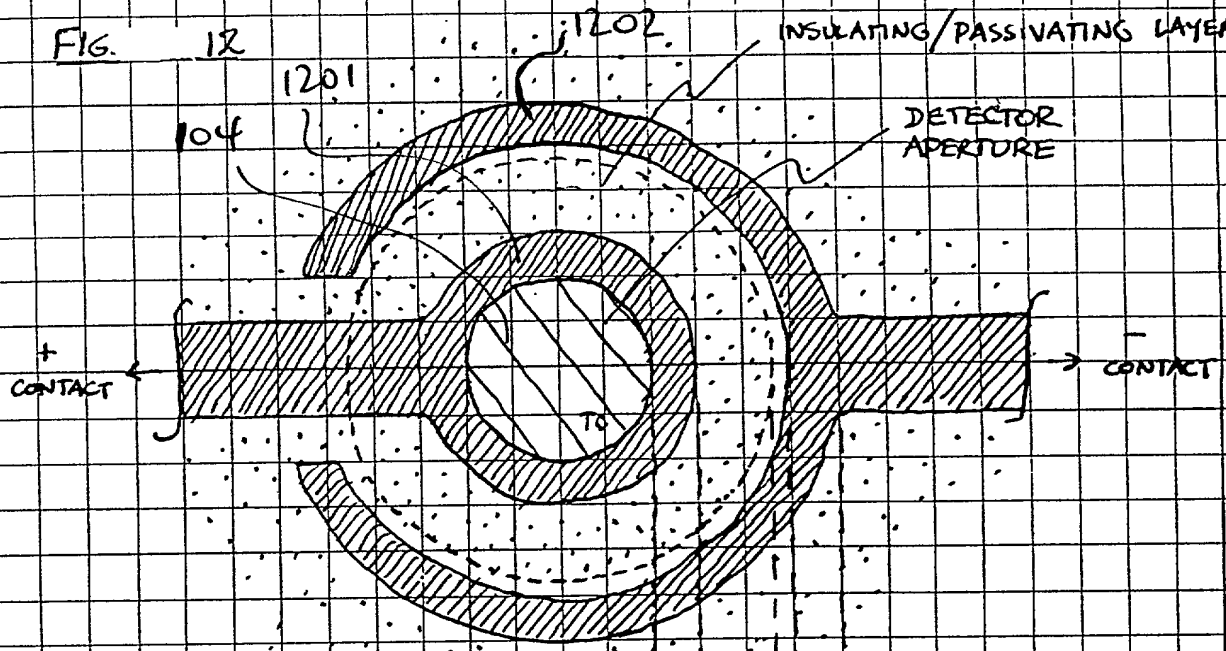
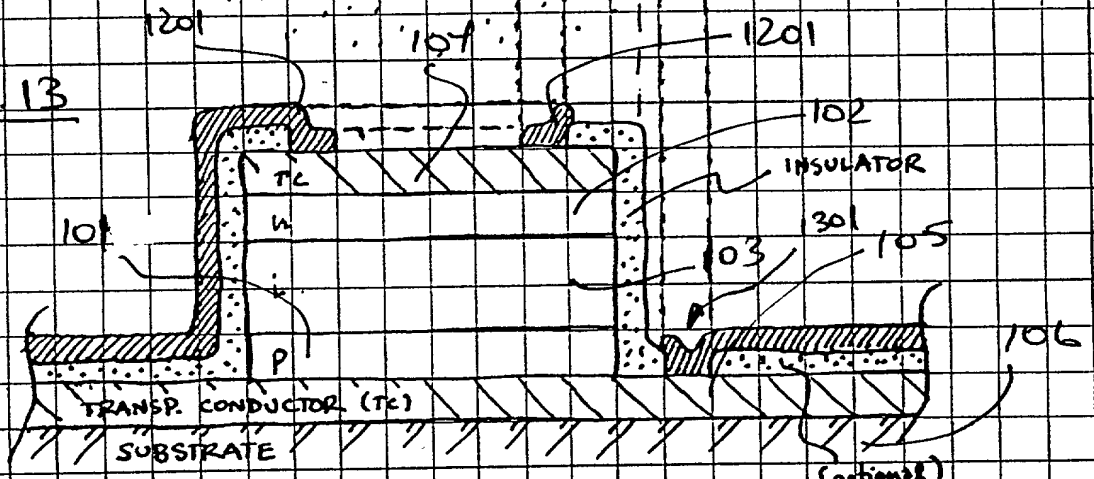


Fig. 13



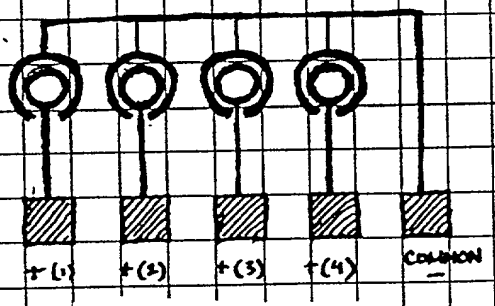


Fig. 14

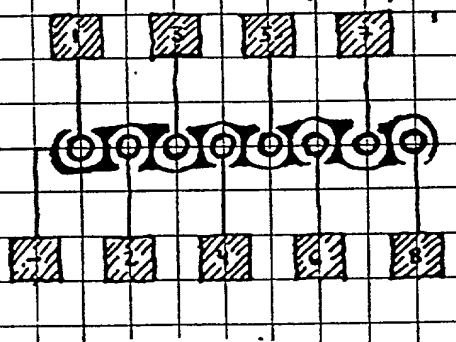
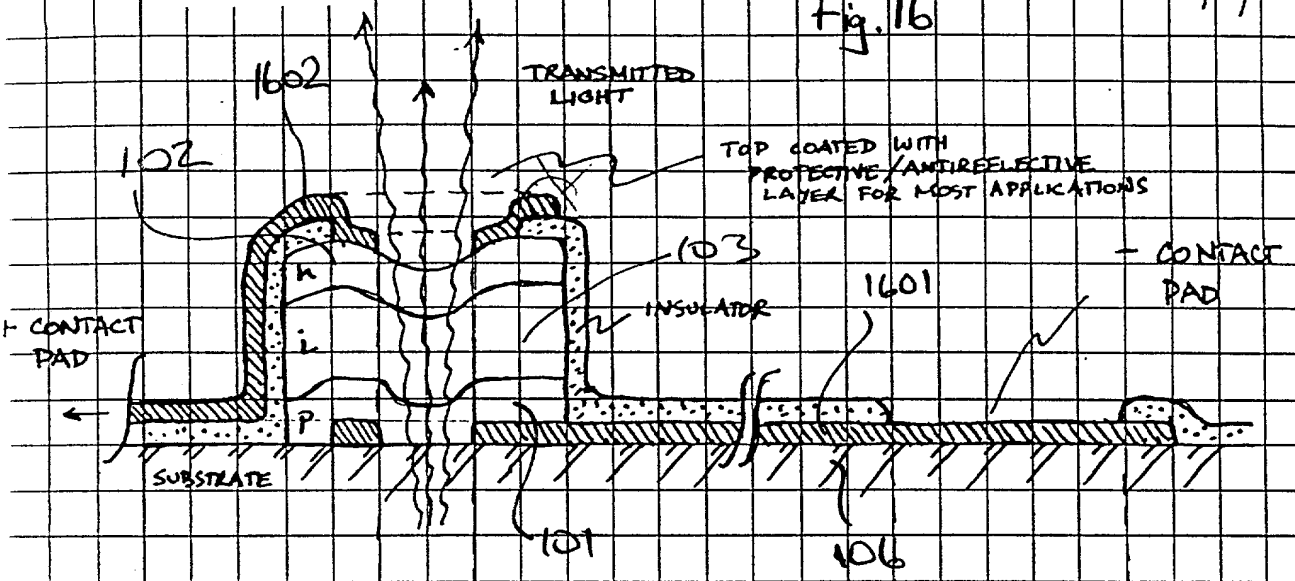


Fig. 15

3/25/00

Fig. 16



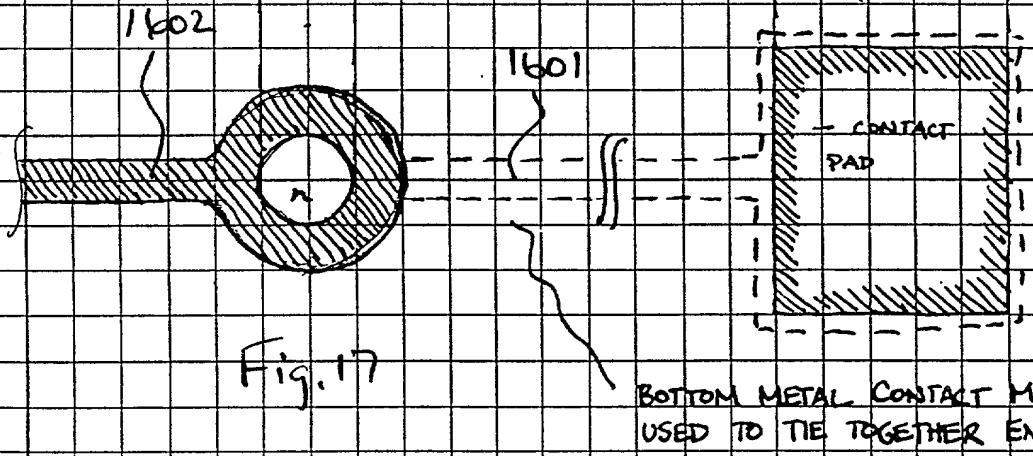


Fig. 17

5/3/00

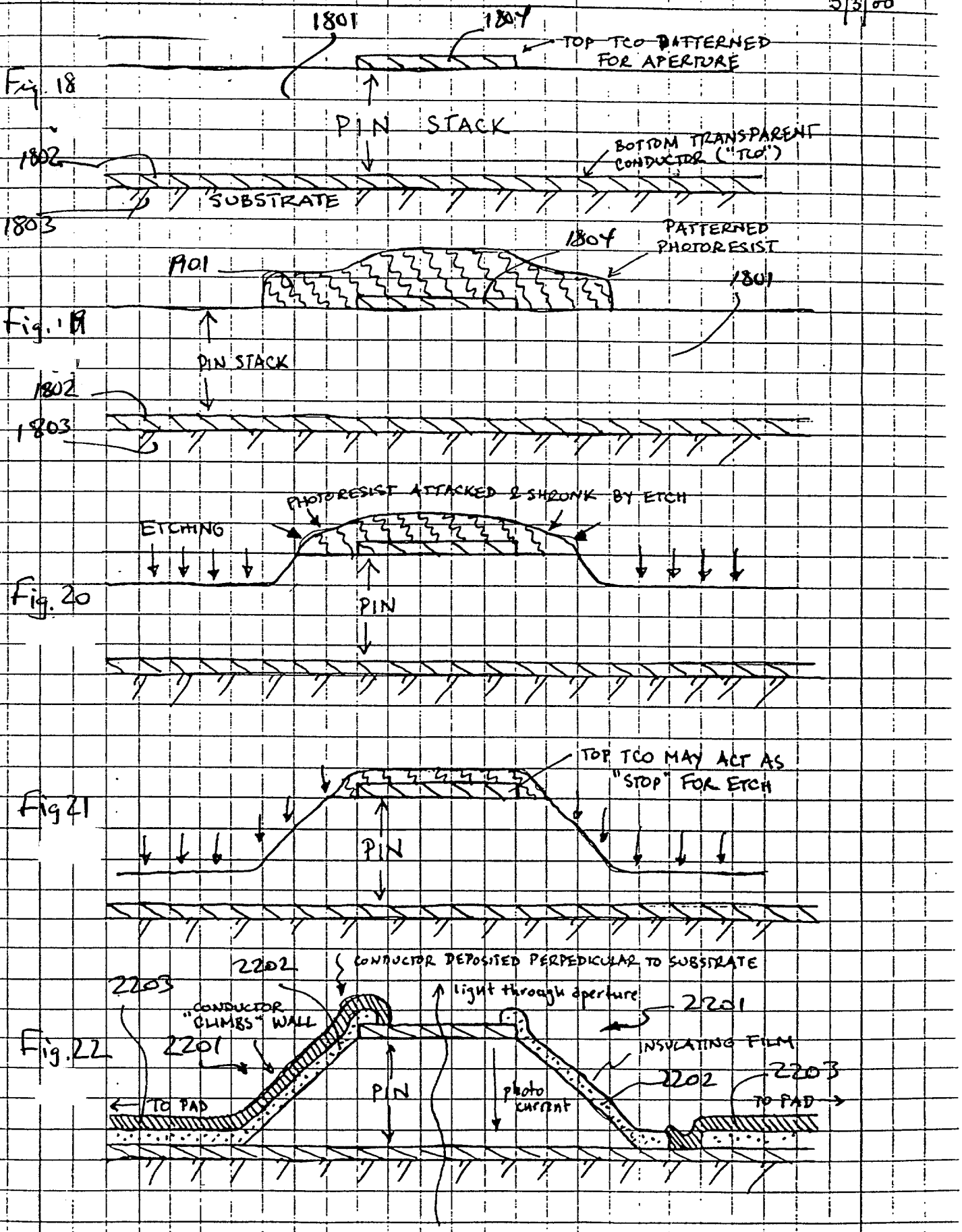


Fig. 18

Fig. 19

Fig. 20

Fig 21

Fig. 22

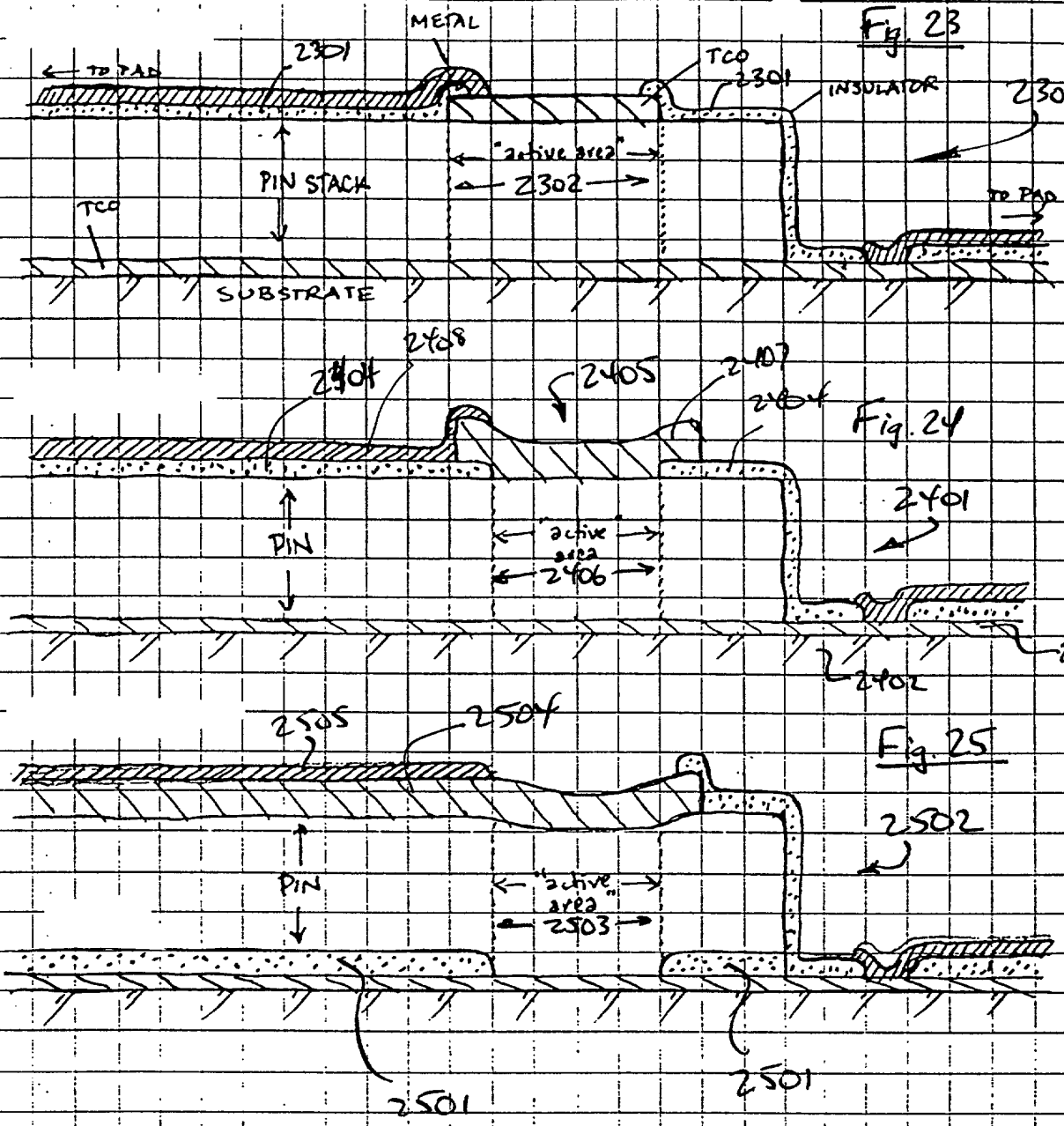


Fig. 23

Fig. 24

Fig. 25

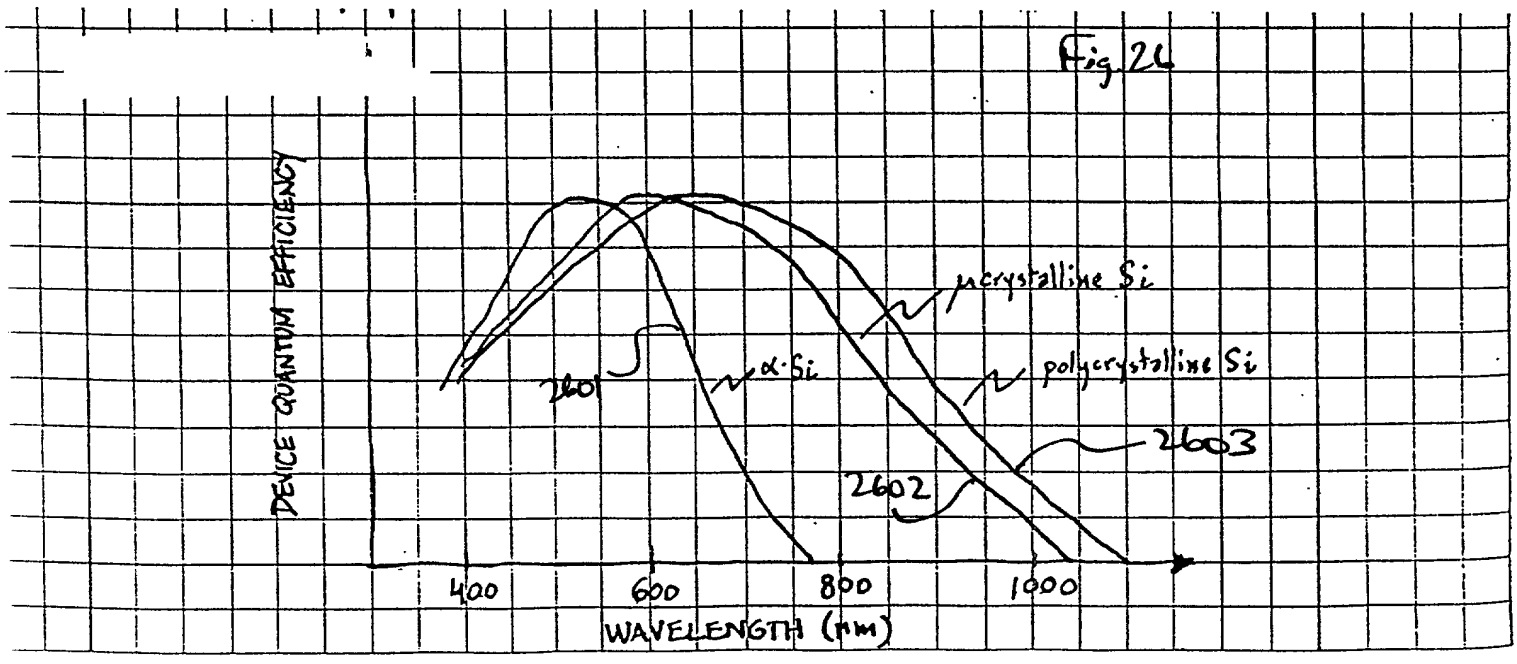

DEVICE QUANTUM EFFICIENCY
400
600
800
1000
WAVELENGTH (nm)
2601
α-Si
microcrystalline Si
polycrystalline Si
2603
2602

Fig. 26

Fig. 27

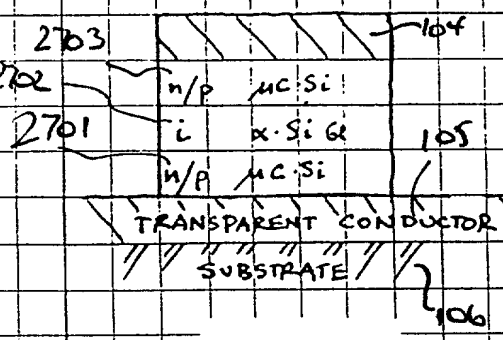


Fig. 28

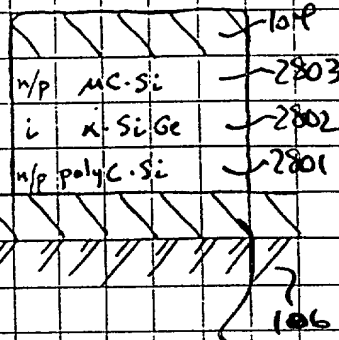
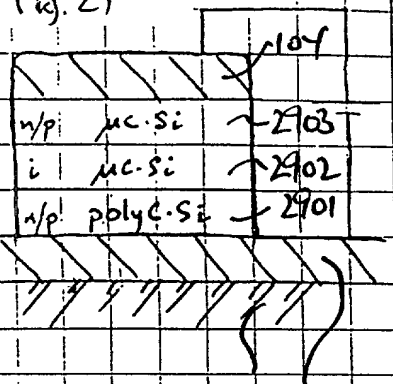


Fig. 29



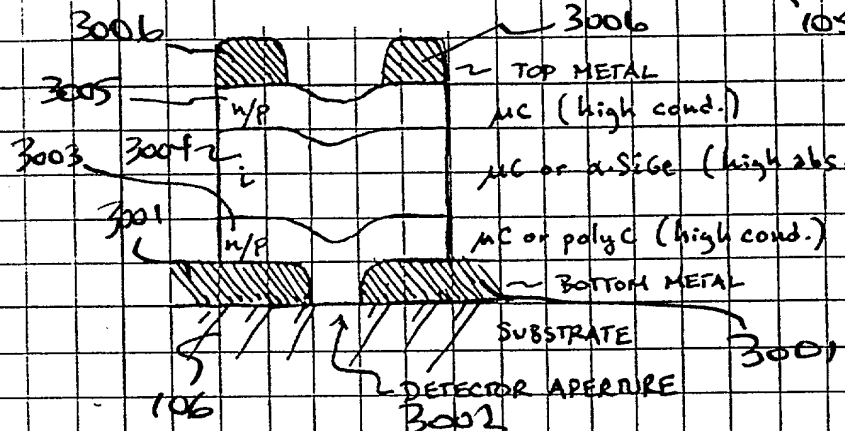


Fig. 30

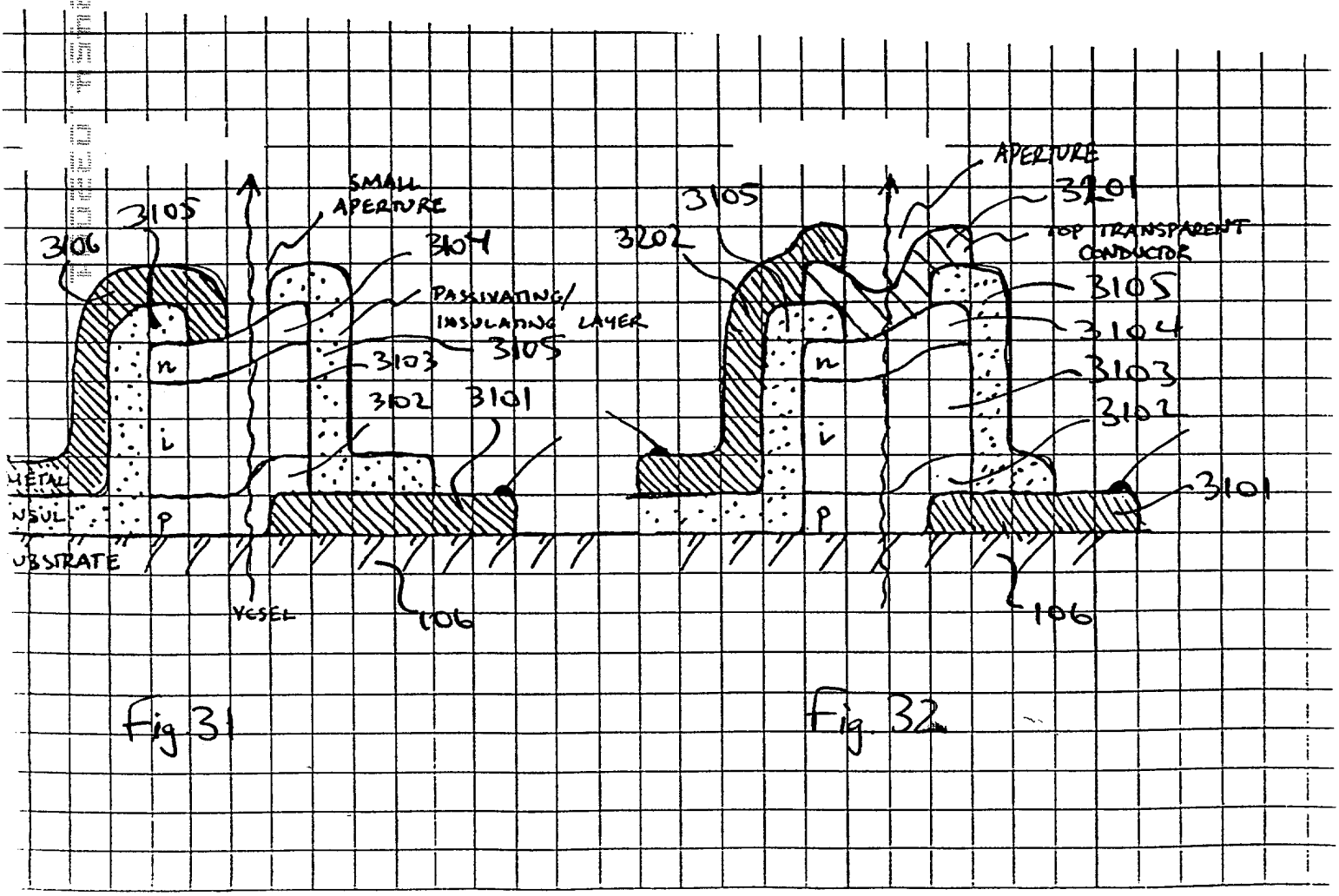

A
SMALL APERTURE
3105
3106
3104
PASSIVATING/ INSULATING LAYER
3103
3105
3102
3101
n
i
p
METAL
INSUL.
SUBSTRATE
VESSEL
106

Fig 31

APERTURE
3101
3105
3202
TOP TRANSPARENT CONDUCTOR
3105
3104
3103
3102
3101
n
i
p
106

Fig 32

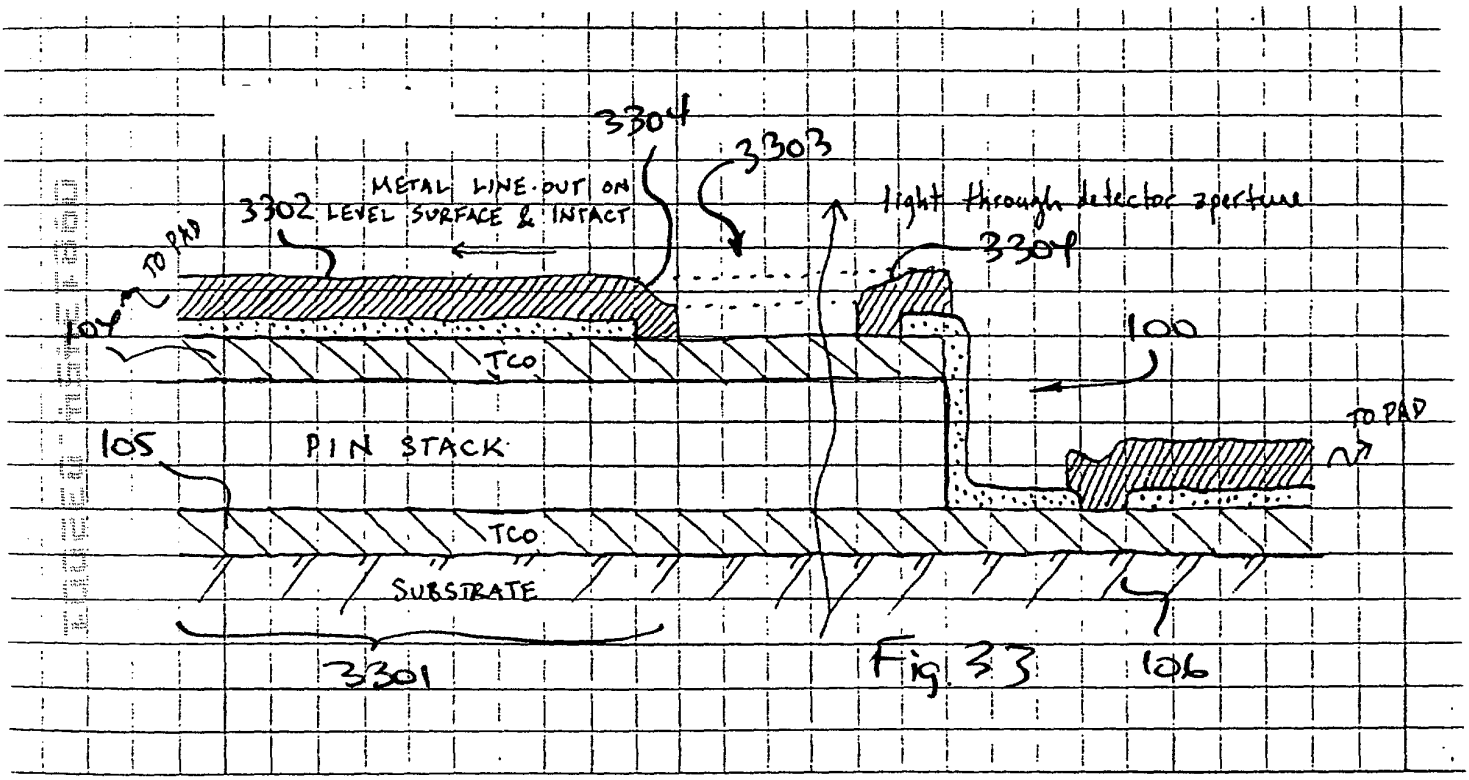
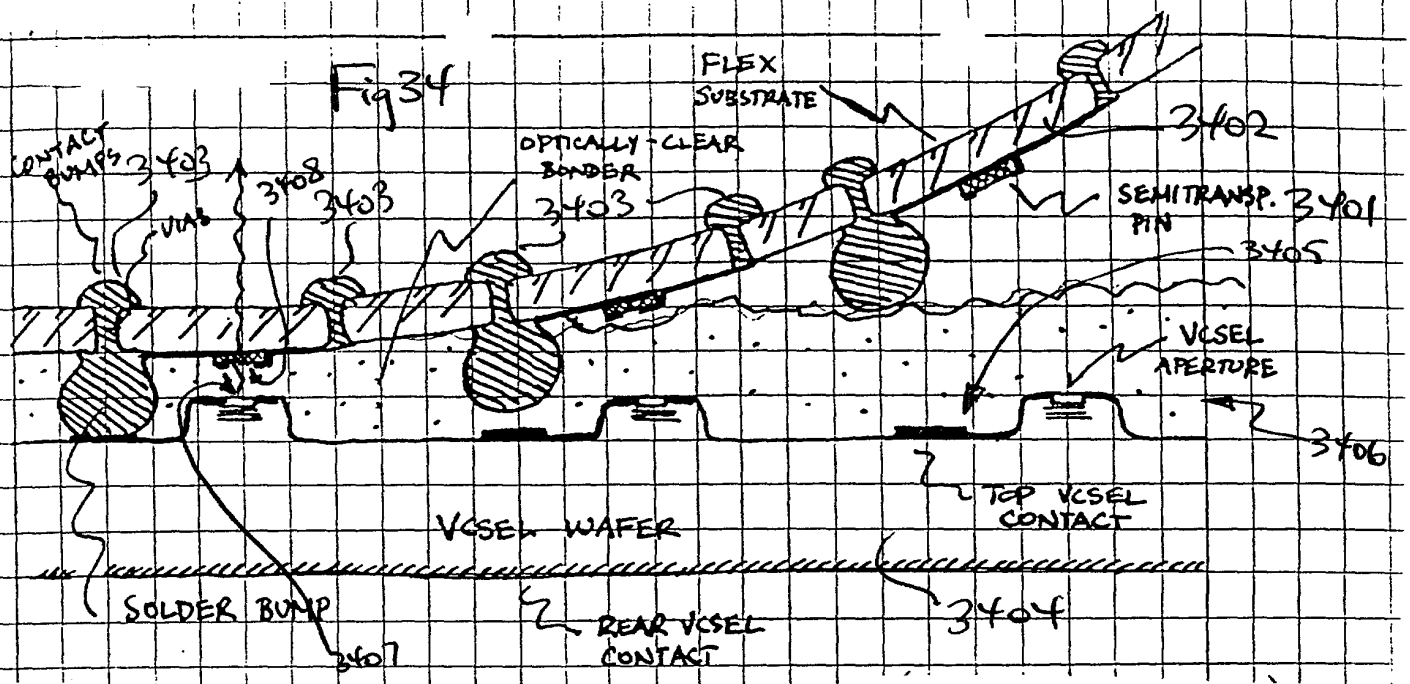

3304
3303
METAL LINE OUT ON LEVEL SURFACE & INTACT
3302
light through detector aperture
3304
TO PAD
104
100
TCO
105
PIN STACK
TO PAD
TCO
SUBSTRATE
3301
106

Fig 33

Fig 34



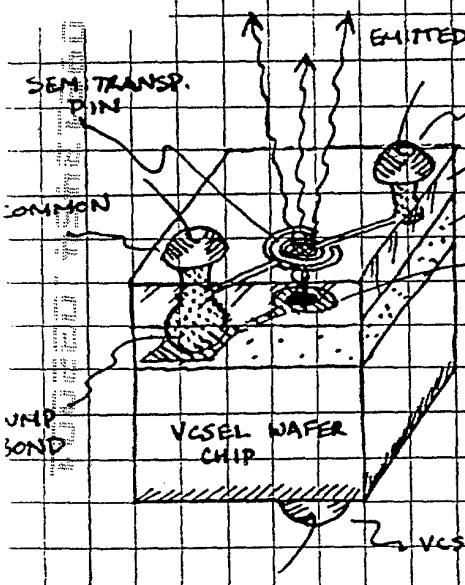


Fig 35

NOTE: ALTERNATIVE CONFIGURATION HAS 3 TOP CONTACTS (NO COMMON); MAY BE PREFERABLE FOR HIGH-SPD. SWITCHING. (PERHAPS EVEN FORM HOLE THROUGH PIN SUBSTRATE & BOND LAYER TO VCSEL TOP CONTACT).

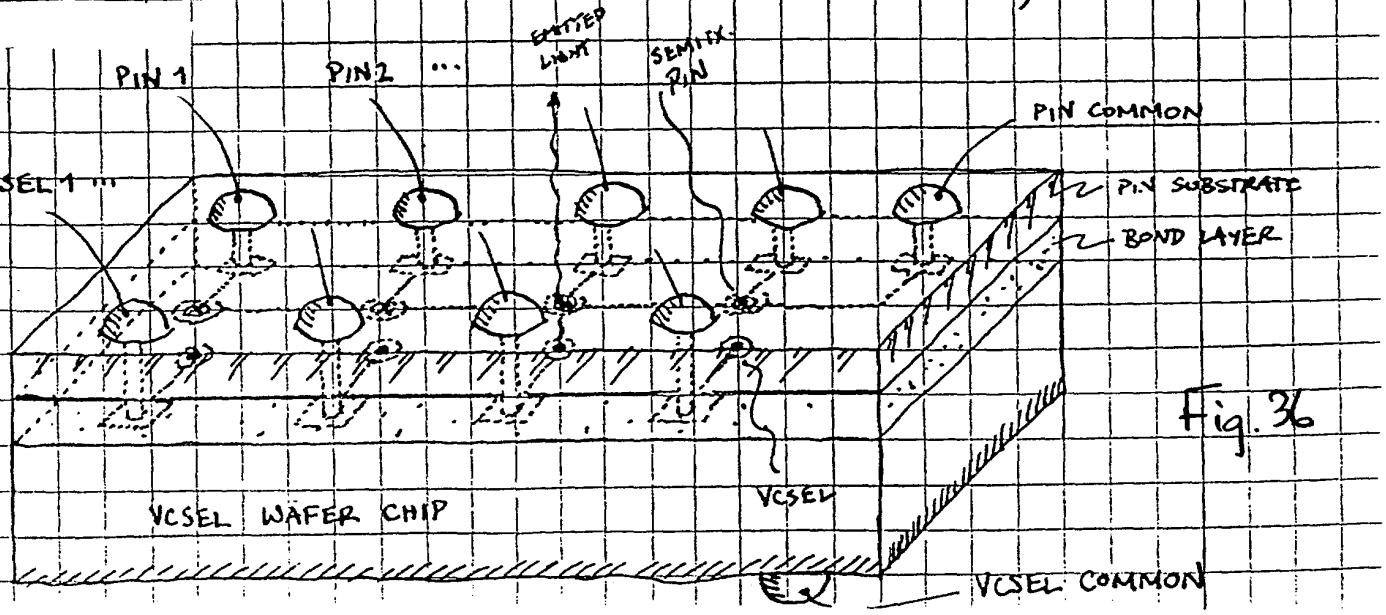


Fig. 36

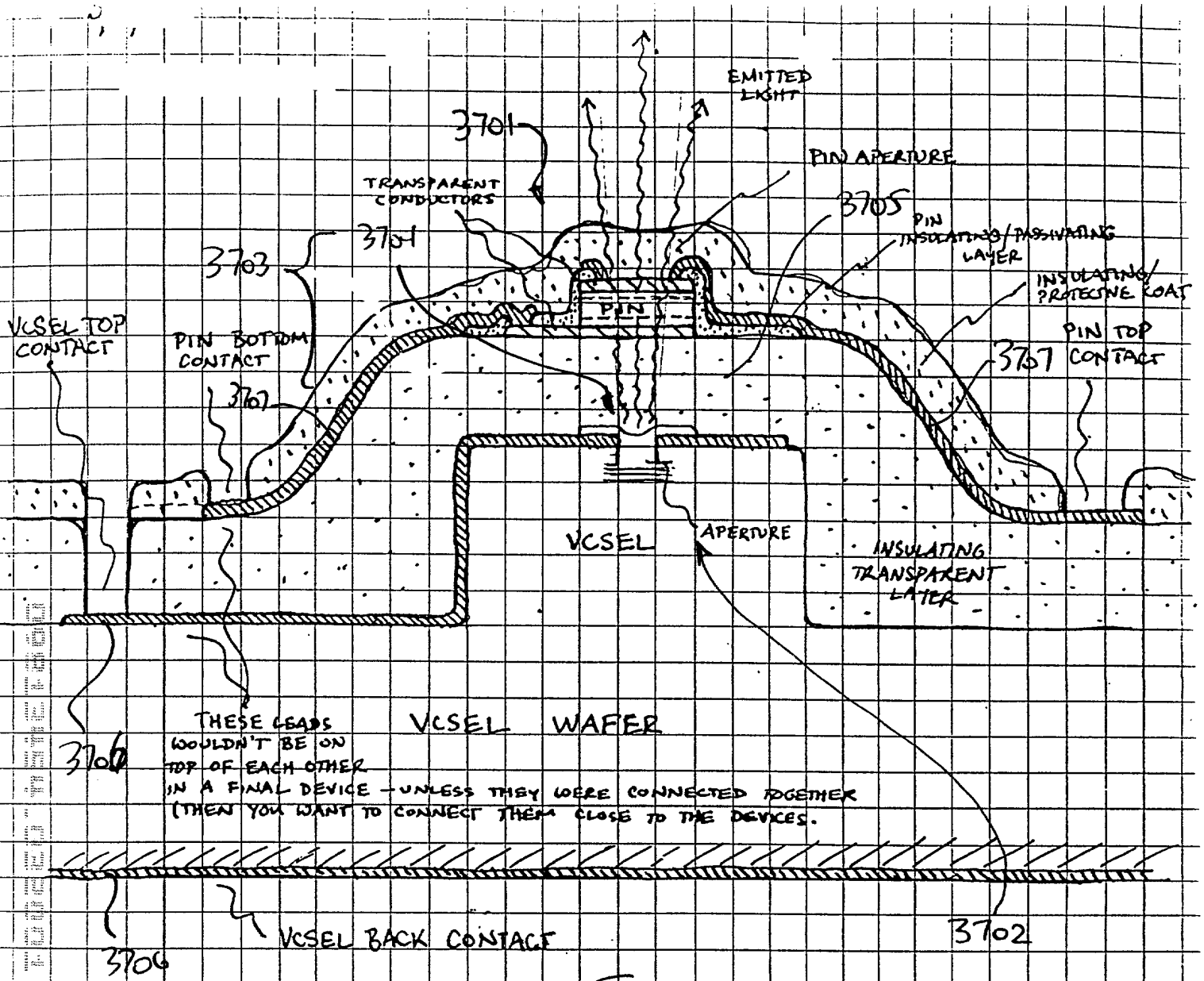

EMITTED LIGHT
3701
PIN APERTURE
TRANSPARENT CONDUCTORS
3705
PIN INSULATING/PASSIVATING LAYER
3704
3703
INSULATING/PROTECTIVE COAT
PIN
VCSEL TOP CONTACT
PIN BOTTOM CONTACT
PIN TOP CONTACT
3707
3707
VCSEL
APERTURE
INSULATING TRANSPARENT LAYER
THESE LEADS WOULDN'T BE ON TOP OF EACH OTHER IN A FINAL DEVICE - UNLESS THEY WERE CONNECTED TOGETHER (THEN YOU WANT TO CONNECT THEM CLOSE TO THE DEVICES.
VCSEL WAFER
3706
VCSEL BACK CONTACT
3702
3706

Fig. 37

3/28/00

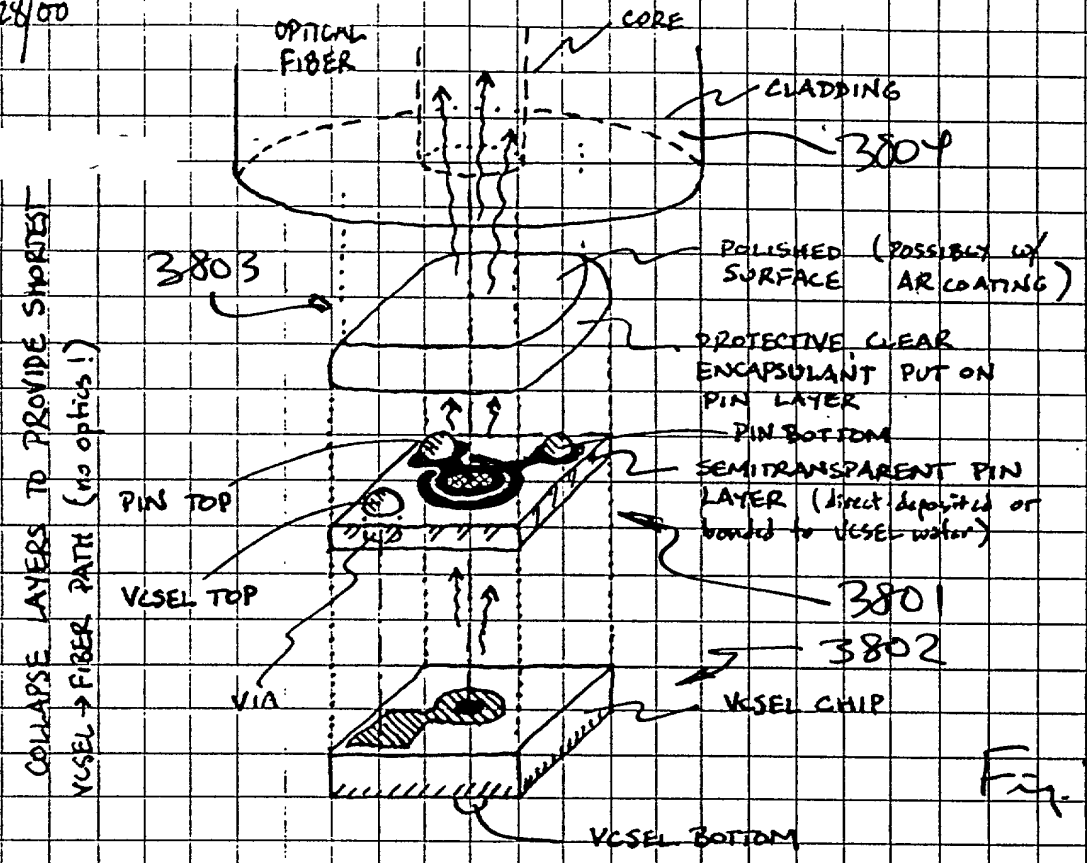


Fig. 38

... SUCH A PACKAGE WOULD ALLOW LOW-COST, DIRECT COUPLING IN A FIBER CONNECTOR (VCSEL APERTURE < 25 μm AND MULTIMODE FIBER CORE ≈ 50-62.5 μm; VCSEL BEAM DIVERGENCE ≤ 20°, AND PIN LAYER IS THIN).

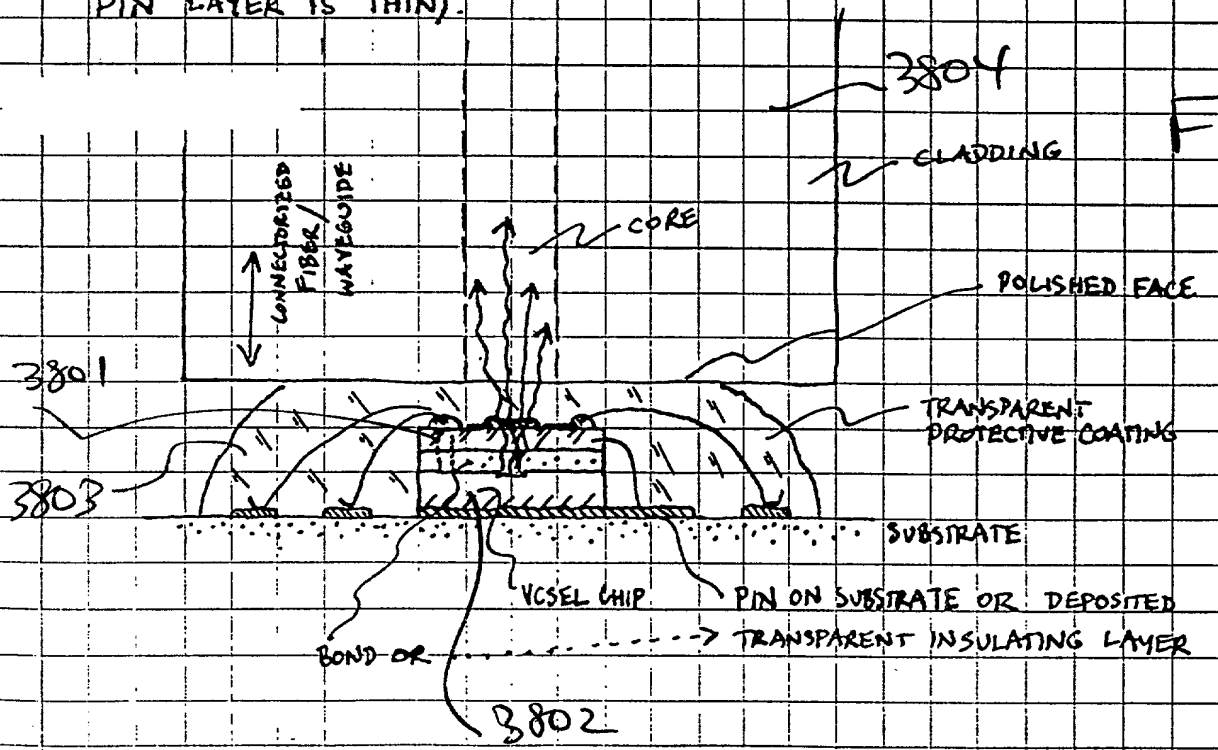
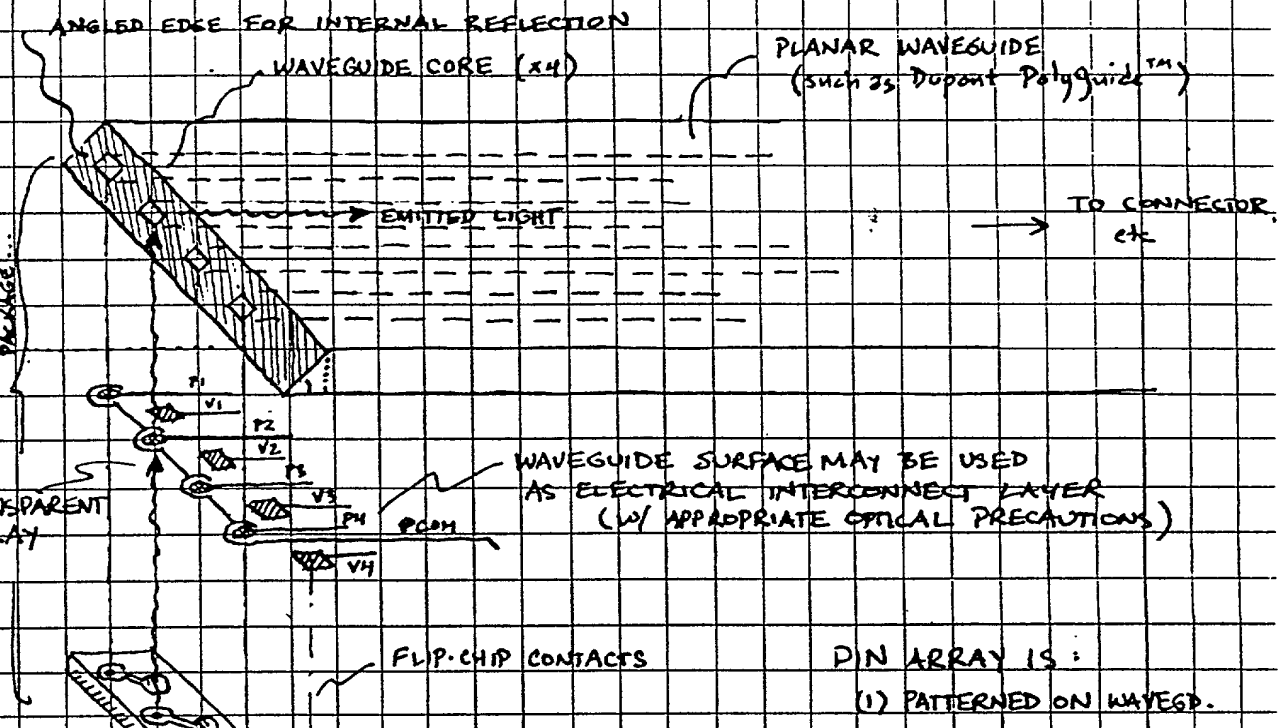
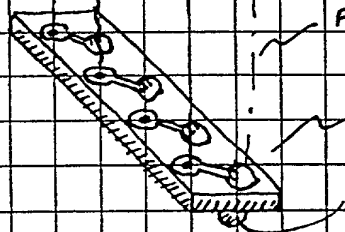


Fig 39

3/28/00

Fig. 40





PIN ARRAY IS:
(1) PATTERNED ON WAVEGD.
(2) PATTERNED ON VCSEL CHIP
OR (3) PATTERNED ON SEPERATE SUBSTRATE

Fig 41

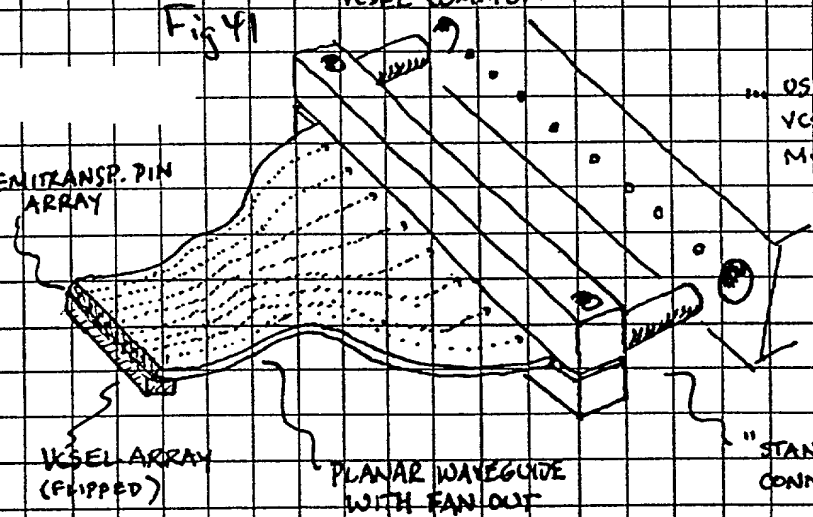


Fig. 42